CLAIMS:

What is claimed is:

1. A method for controlling a plurality of I/O devices being attached to a microprocessor by a special number and type of interfaces comprising:

connecting a configurable chip to the I/O space of said microprocessor, said configurable chip having a switch matrix;

initializing said I/O devices; and

assigning to said switch matrix, said special number and type of interfaces to each I/O device during said initialization.

2. The method according to claim 1, wherein said configurable chip is an active element.

3. The method according to claim 2, wherein said configurable chip is a controller.

4. The method according to claim 1, wherein said configurable chip is a passive element.

5. The method according to claim 4, wherein said configurable chip is an ASIC.

6. The method according to claim 1, wherein said I/O devices support different I/O protocols.

7. The method according to claim 6, wherein said different I/O protocols comprise IC bus (I^2C), Universal Asynchronous Receiver/Transmitter (UART), General Purpose I/O (GPI/O) protocols.

8. The method according to claim 1, wherein said switch matrix is adapted to assign I/O pins according to the needs of each I/O device.

9. The method according to claim 1 further comprising switching in hardware using ID bits on each I/O device.

10. The method according to claim 1, wherein each I/O device contains configuration data.

11. The method according to claim 10, wherein said configuration data includes an identifier for each of said I/O devices.

12. The method according to claim 10, wherein said configuration data includes initialization data.

13. The method according to claim 12, wherein said configuration data is stored in an SEEPROM on said I/O device.

14. The method according to claim 11, wherein said identifier is transmitted to said configurable chip.

15. The method according to any one of claims 9 wherein said switching is done by software initialization.

16. The method according to claim 15, wherein said microprocessor sets up said chip prior to any control task with regard to the device to be controlled.

17. The method according to claim 16, wherein said set up is done by the software identifying each specific device.

18. The method according to claim 16, wherein initialization of said specific device is done after said set up.

19. The method according to claim 1 wherein said initialization is started each time a new I/O device is attached to said microprocessor.

20. The method according to claim 19, wherein said new I/O device is hot plugged to a system.

21. The method according to claim 20, wherein hot plugging is indicated by an interrupt.

22. A computer system comprising:

a microprocessor for controlling I/O devices;

a plurality of I/O devices attached to said microprocessor by a special number and type of interfaces;

a configurable chip connected to the I/O space of said microprocessor, said configurable chip having a switch matrix;

an initializing program initializing one of said I/O devices; and

said initializing program assigning to said switch matrix, said special number and type of interfaces to each I/O device during said initialization.

23. The system according to claim 22, wherein said configurable chip is an active element.

24. The system according to claim 23, wherein said configurable chip is a controller.

25. The system according to claim 22, wherein said configurable chip is a passive element.

26. The system according to claim 25, wherein said configurable chip is an ASIC.

27. The system according to claim 22, wherein said I/O devices support different I/O protocols.

28. The system according to claim 27, wherein said different I/O protocols comprise IC bus (I^2C), Universal Asynchronous Receiver/Transmitter (UART), General Purpose I/O (GPI/O) protocols.

29. The system according to claim 22, wherein said switch matrix is adapted to assign I/O pins according to the needs of each I/O device.

30. The system according to claim 22 further comprising switching in hardware using ID bits on each I/O device.

31. The system according to claim 22, wherein each I/O device contains configuration data.

32. The system according to claim 31, wherein said configuration data includes an identifier for each of said I/O devices.

33. The system according to claim 31, wherein said configuration data includes initialization data.

34. The system according to claim 33, wherein said configuration data is stored in an SEEPROM on said I/O device.

35. The system according to claim 32, wherein said identifier is transmitted to said configurable chip.

36. The system according to any one of claims 30 wherein said switching is done by software initialization.

37. The system according to claim 36, wherein said microprocessor sets up said chip prior to any control task with regard to the device to be controlled.

38. The system according to claim 37, wherein said set up is done by the software identifying each specific I/O device.

39. The system according to claim 37, wherein initialization of said specific device is done after said set up.

40. The system according to claim 22, wherein said initialization is started each time a new I/O device is attached to said microprocessor.

41. The system according to claim 40, wherein said new I/O device is hot plugged to a system.

42. The system according to claim 41, wherein hot plugging is indicated by an interrupt.

43. A program product for controlling a plurality of I/O devices being attached to a microprocessor by a special number and type of interface and having a generic configurable chip connected to the I/O space of the microprocessor, the configurable chip having a switch matrix, said program product comprising:

a computer readable medium having recorded thereon computer readable program code performing the method comprising:

initializing said I/O devices; and

assigning to said switch matrix, said special number and type of interfaces to each I/O device during said initialization.

44. The program product according to claim 43, wherein said I/O devices support different I/O protocols.

45. The program product according to claim 44, wherein said different I/O protocols comprise IC bus (I^2C), Universal Asynchronous Receiver/Transmitter (UART), General Purpose I/O (GPI/O) protocols.

46. The program product according to claim 43 further comprising switching in hardware using ID bits on each I/O device.

47. The program product according to claim 43, wherein each I/O device contains configuration data.

48. The program product according to claim 47, wherein said configuration data includes an identifier for each of said I/O devices.

49. The program product according to claim 47, wherein said configuration data includes initialization data.

50. The program product according to claim 49, wherein said configuration data is stored in an SEEPROM on said I/O device.

51. The program product according to claim 48, wherein said identifier is transmitted to said configurable chip.

52. The program product according to any one of claims 46 wherein said switching is done by software initialization.

53. The program product according to claim 52, wherein said microprocessor sets up said chip prior to any control task with regard to the device to be controlled.

54. The program product according to claim 53, wherein said set up is done by the software identifying each specific device.

54. The program product according to claim 53, wherein initialization of said specific device is done after said set up.

55. The program product according to claim 43 wherein said initialization is started each time a new I/O device is attached to said microprocessor.

56. The program product according to claim 55, wherein said new I/O device is hot plugged to a system.

57. The program product according to claim 56, wherein hot plugging is indicated by an interrupt.